

Anuj Mishra

SILICON DESIGN ENGINEER 2, ADVANCED MICRO DEVICES

☎ (+91) 8861489598 | ✉ mishraanuj.cs@gmail.com | 📱 mishraanuj03

Experience

Silicon Design Engineer 2 ADVANCED MICRO DEVICES

Dec 2021 - Present

- Did extensive experiments and tuned all prefetchers, to provide 1.5% and 2.6% perf uplift on SPEC FP and SPEC INT.
- Investigated prefetch throttling tuning thresholds, identified and disseminated the optimal tuning configuration, which was subsequently forwarded to our customers as official AMD recommendations.
- Collaborated with the workload tracing team to gather and correlate genuine NT traces for the SPEC 2017 benchmark suite.
- Tuned different SOC features like Priority escalation, Adaptive Allocation and Latency Under Load for best performance.
- Partnered with the infrastructure team to develop a widely utilized tool for conducting triages and reporting causes of low simulator health.
- Regularly conducted data sharing regressions, identified causes for low simulator health, debugged the associated errors, and collaborated with different IP teams to resolve bugs.
- Became the owner for cache to cache latency and bandwidth analysis. Created tests, built additional infra to optimize simulation runtime, did performance analysis, silicon and RTL correlation, competitive analysis.

Developer Intern CLASSCALC, LOS ANGELES

Jan.2018- Sep. 2018

- Worked as a remote intern to add new UI features and add-ons in their cross-platform application as well as find and fix bugs in their code-base.

Publications

Anuj Mishra, Biswabandan Panda, "Hardware Prefetcher Aggressiveness Controllers: Do We Need Them All the Time?", in 5th Workshop on Negative results, Opportunities, Perspectives, and Experiences (NOPE 2021) co-located with ASPLOS-26, April 2021

Projects

Cross core conflict attack detectors COURSE PROJECT WITH DR. BISWABANDAN PANDA

Oct. 2019 - Nov. 2019

- Used ChampSim to apply different techniques for restricting cross core evictions to prevent Eviction based attacks with minimum performance degradation. Devised new attack patterns for the proposed method and implemented mitigations.

Cache Based Attacks COURSE PROJECT WITH DR. BISWABANDAN PANDA

Aug 2019 - Sep. 2019

- Implemented Flush+Reload attack in ChampSim to create a side-channel for attacking the GNU PG library and extract RSA keys.
- Used Flush+Reload attack to transfer text and Image files by creating a cache covert channel.

Linux Kernel Driver Implementation COURSE PROJECT WITH DR. DEBADATTA MISHRA

Feb 2020 - March 2020

- Implemented a device driver for a PCI device CryptoCard which performs encryption/decryption of data, provided support for MMIO and DMA data transfers with interrupts and polling for event handling.
- Implemented a user-space library to allow end users to access device.

CryptoBox COURSE PROJECT WITH DR. PRAMOD SUBRAMANYAM

Oct. 2019 - Nov 2019

- Implemented a secure file server in Golang. Learnt and implemented different crypto primitives that allow users to save their files on a non-trusted server. Implemented file sharing among users and tested the server for different possible attacks.

Parallel K-Means clustering algorithm using MPICH COURSE PROJECT WITH DR. PREETI MALAKAR

Aug 2019 - Sep. 2019

- Used MPI library to parallelise and speed up the clustering and evaluated the scalability on CSE and HPC clusters at IITK.

Education

2019 - 2021	MS(Research) (Computer Science & Engineering)	Indian Institute of Technology, Kanpur	9.5/10
2015 - 2019	B.Tech. (Computer Science & Engineering)	Ambalika Institute of Management and Technology	78.55%
2014-2015	Class 12 th (CBSE)	Bal Vidya Mandir, Lucknow	90.2%
2012-2013	Class 10 th (CBSE)	Bal Vidya Mandir, Lucknow	92%

Achievements

2020	Received Academic excellence award at , IIT Kanpur	<i>IIT Kanpur</i>
2019	Worked on SRC funded research project with Intel, Under the guidance of Prof. Biswabandan Panda	<i>IIT Kanpur</i>

Skills

Programming C/C++, Python, JavaScript

Utilities ChampSim, Bash, Git, GDB, Vim, LaTeX, Intel VTune, AMD uProf